CLAIMS

1. A transistor substrate for a liquid crystal display comprising: a substrate; a transistor over the substrate, the transistor comprising an insulated-gate staggered structure having substantially coplanar source and drain regions and a gate region, a gate insulator lying between the gate region and the source and drain regions; and a capacitor associated with the transistor and lying adjacent the transistor, the capacitor comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator comprises a first inorganic layer and a second, polymer or spin-on glass layer, of which layers only the polymer or spin-on glass layer extends to the capacitor to define the capacitor dielectric.

2. A transistor substrate as claimed in claim 1, wherein the polymer or spin-on glass layer comprises polyimide.

3. A transistor substrate as claimed in claim 1 or 2, wherein the transistor comprises a top gate transistor.

4. A liquid crystal display comprising a plurality of pixels provided over a transistor substrate as claimed in any preceding claim, each pixel comprising a respective transistor and capacitor, and wherein the thicknesses of the first and second layers are selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second polymer or spin-on glass layer defining the capacitor dielectric.

5. A liquid crystal display as claimed in claim 4, wherein, each pixel comprises a capacitor of capacitance C_{store} and is associated with liquid crystal material having a capacitance C_{LC} , wherein the thickness of the inorganic layer d_{inorg} and the thickness of the polymer or spin-on glass layer d_{poly} are selected approximately to satisfy the relation:

$d_{poly} = (C_{store}/C_{LC}) . (\varepsilon_{poly}/\varepsilon_{inorg}) . d_{inorg}$

in which ε_{poly} and ε_{inorg} are the permittivity constants of the polymer or spin-on glass layer and the inorganic layer, respectively.

6. A liquid crystal display comprising a plurality of pixels each comprising a switching transistor, a storage capacitor of capacitance C_{store}, and liquid crystal material of capacitance C_{LC}, the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions and a gate region, a gate insulator lying between the gate region and the source and drain regions, the capacitor comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator comprises first and second layers, of which layers only the second extends to the capacitor to define the capacitor dielectric, and wherein the thicknesses of the first and second layers are selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

7. A display as claimed in claim 6, wherein the thickness of the first layer d_1 and the thickness of the second layer d_2 are selected approximately to satisfy the relation:

$d_2 = (C_{store}/C_{LC}) . (\varepsilon_2/\varepsilon_1) . d_1$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers, respectively.

8. A display as claimed in claim 6 or 7, wherein the first layer comprises an inorganic layer, and the second layer comprises a polymer or spin-on glass layer.

9. A display as claimed in claim 8, wherein the second layer comprises polyimide.

10. A method of manufacturing a transistor substrate for a liquid crystal display, comprising: providing an array of transistors and capacitors over the substrate, the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions and a gate region, a gate insulator lying between the gate region and the source and drain regions; and the capacitors comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator is deposited as first and second layers, a first layer being deposited by vacuum deposition process, and a second layer being deposited by a non-vacuum process, the first layer being patterned to remove it from areas corresponding to the capacitors, and the second layer extending to the areas corresponding to the capacitors to define the capacitor dielectric.

11. A method of manufacturing a liquid crystal display, comprising manufacturing a transistor substrate using the method of claim 8, and providing liquid crystal material over the transistor substrate, wherein the first insulator is deposited to a thickness d_1, and the second layer is deposited to a thickness d_2, the thicknesses being selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

12. A method as claimed in claim 11, wherein the capacitors have capacitance C_{store} and each pixel is associated with liquid crystal material of capacitance C_{LC}, and wherein the thickness of the first layer d_1 and the thickness of the second layer d_2 are deposited to depths selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}) \,.\, (\varepsilon_2/\varepsilon_1) \,.\, d_1$$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers, respectively.